CLAIMS

What is claimed is:

1. A method for fabricating a memory device comprising:

depositing a dopant in a first region of a semiconductor substrate of a memory device;

performing an annealing process upon said semiconductor substrate;

performing a second depositing of a dopant in a second region of said semiconductor substrate; and

performing a second annealing process upon said semiconductor substrate.

2. The method as recited in Claim 1, wherein said depositing a dopant comprises creating an impurity concentration in a semiconductor substrate of a flash memory device.

3. The method as recited in Claim 1, wherein said depositing a dopant comprises depositing a dopant for a plurality of semiconductor devices in a periphery region of said memory device.

4. The method as recited in Claim 3, wherein said performing a second depositing comprises depositing a dopant for a plurality of memory cells in a core region of said semiconductor substrate of said memory device.

5. The method as recited in Claim 4, wherein a plurality of parameters of said second annealing process are selected based upon an electrical characteristic of said plurality of memory cells.

6. The method as recited in Claim 5, wherein said annealing process and said second annealing process comprise a cumulative annealing process for said plurality of semiconductor devices.

7. The method as recited in Claim 6, wherein a plurality of parameters of said cumulative annealing process are selected based upon an electrical characteristic of said plurality of semiconductor devices.

8. A method for fabricating a flash memory device comprising:

performing a partial annealing process upon a dopant deposited in a first region of a semiconductor substrate of said flash memory device;

depositing a dopant in a second region of said semiconductor substrate; and

performing a second annealing process wherein said dopant deposited in said first region and said dopant deposited in said second region are simultaneously annealed.

9. The method as recited in Claim 8, wherein said first region comprises a plurality of semiconductor devices disposed in a periphery region of said flash memory device and comprising performing a partial annealing process upon said plurality of semiconductor devices.

10. The method as recited in Claim 9, wherein said second region comprises a plurality of memory cells disposed in a core region of said flash memory device and comprising performing a partial annealing process upon said plurality of memory cells.

11. The method as recited in Claim 10, wherein a plurality of parameters of said second annealing process are selected based upon an electrical characteristic of said plurality of memory cells.

12. The method as recited in Claim 11, wherein a plurality of parameters of said partial annealing process are selected based upon an electrical characteristic of said plurality of semiconductor devices and upon said plurality of parameters of said second annealing process.

13. A method for fabricating a memory device comprising:

initiating a partial diffusion of a dopant deposited in a first region of a semiconductor substrate of a memory device;

depositing a dopant in a second region of said semiconductor substrate; and

initiating a second diffusion wherein said dopant in said first region is further diffused concurrent with the diffusion of said dopant in said second region.

14. The method as recited in Claim 13, wherein said memory device comprises a flash memory device.

15. The method as recited in Claim 13, wherein said first region comprises a plurality of semiconductor devices disposed in a periphery region of said memory device.

16. The method as recited in Claim 15, wherein said second region comprises a plurality of memory cells disposed in a core region of said memory device.

17. The method as recited in Claim 16, wherein a plurality of parameters of said second diffusion are selected based upon an electrical characteristic of said plurality of memory cells.

18. The method as recited in Claim 17, wherein said partial diffusion and said second diffusion comprise a cumulative diffusion for said plurality of semiconductor devices.

19. The method as recited in Claim 18, wherein a plurality of parameters of said cumulative diffusion are selected based upon an electrical characteristic of said plurality of semiconductor devices.